Learning Control Applied to a Digital-to-analogue Converter

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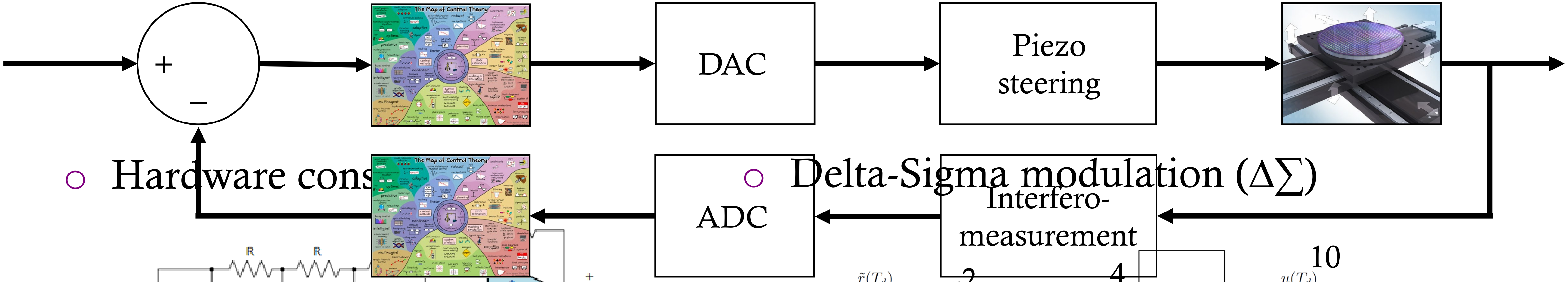
Noa van Rijt (TU/e)
Ahmad Faza (UiS)
Tom Oomen (TU/e)
Arnfinn A. Eielsen (UiS)

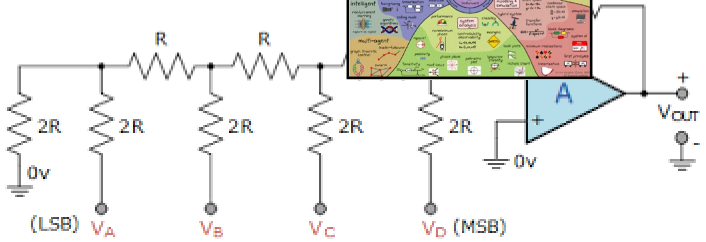
Universitetet i Stavanger

TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

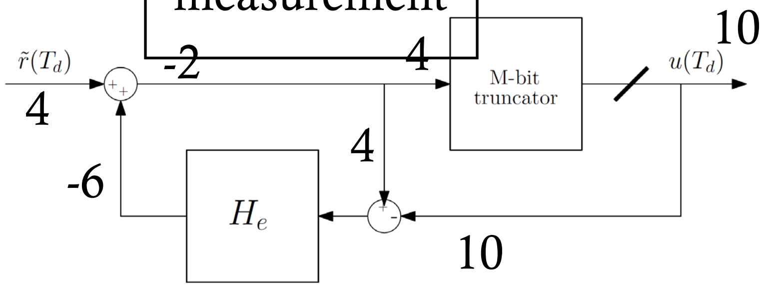
Motivation for Ultra Linear DACs in High Precision Applications



- Hardware cons

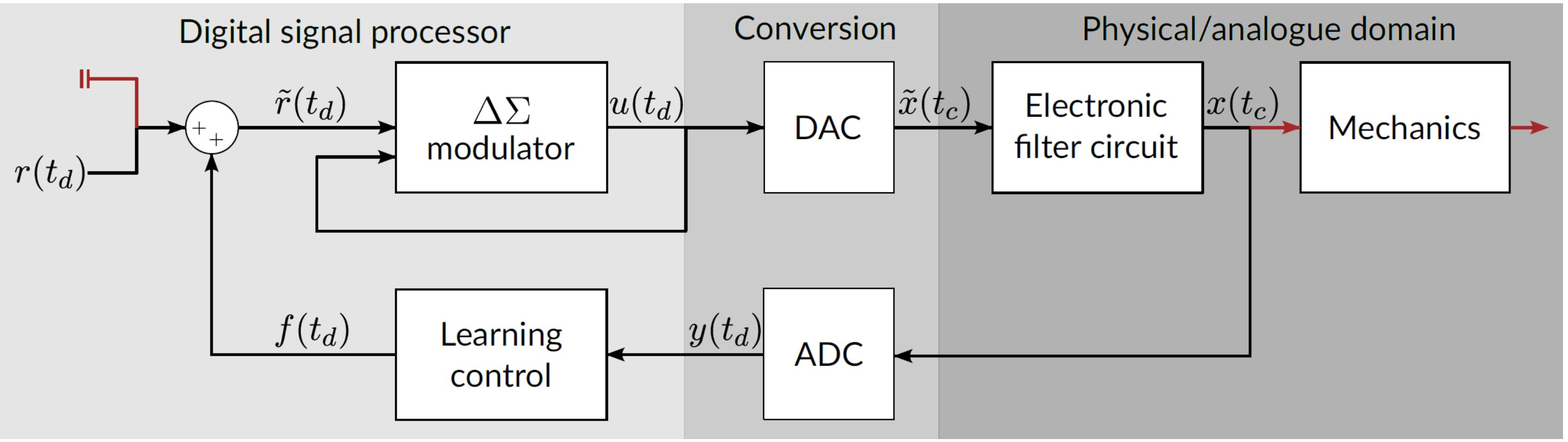


- Delta-Sigma modulation (Δ∑)



- System characteristics
  - Quantization intervals
  - Integral non-linearity
  - Transistor distortions
- Control methodologies
  - Model compensation
  - Dither and filtering
  - Feedback control? — Traditional > OL observer FB! / MPC > computationally intensive!

System Framework

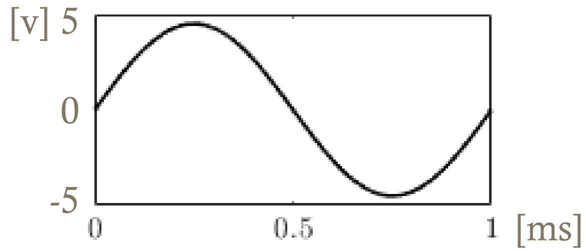


- Why applying ILC to a DAC
  - Phase response of the Anti-aliasing/ reconstruction filter is incorporated as the plant (avoids phase margin limitation when utilizing ADCs for FB)
  - Removes all invariant errors
  - Unique gap in the literature allowing the use of classical FB control

Research question:

Can learning control improve the performance from a digital-to-analogue converter over traditional Delta-Sigma modulation without using complex calibrated methods?

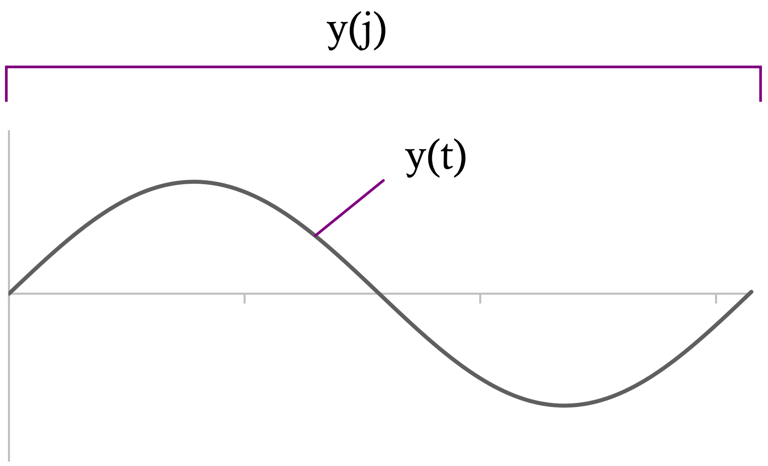
- Relative RMSE performance: ΔΣ + DAC VS ΔΣ + DAC + LC.

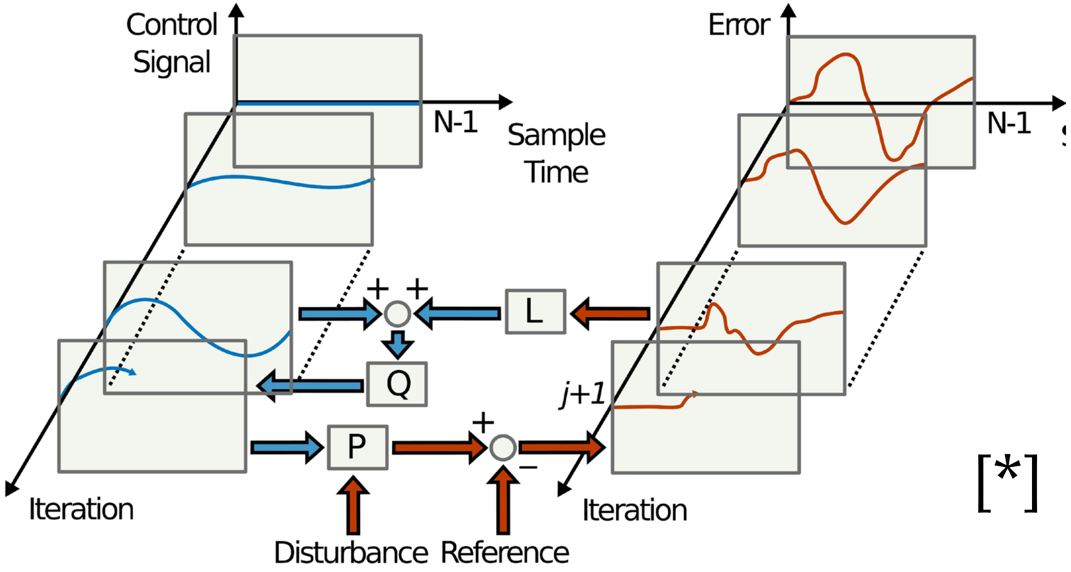


Background information on (I)LC

[*] F. Queißer. Multi-modal Skill Memories for Online Learning of Interactive Robot Movement Generation. Bielefeld: Universität Bielefeld, 201

- What is (Iterative) Learning Control?
  - Technique that operates on complete experiment signals: u(j) and e(j).
  - Traditional FB or OL experiments are run online, and the error trajectory is saved for offline data processing.
  - As the invariant error trajectories are predictable, they can be feedback into temporal feedforward control actions.
  - This process is performed iteratively or repetitively (with or without reset)





[*]

Implementing Learning Control

Update rule for a reference-augmenting feed-forward element f

$$f(j+1) = Q * f(j) + L * e(j)$$

A norm-optimal feedforward is achieved if the cost function J is minimised

$$J(f_j) = e_j^T W_e e_j + f_j^T W_f f_j + (f_j - f_{j-1})^T W_{\Delta F}(f_j - f_{j-1})$$

Accordingly, for $I = (G^T W_e G + W_f + W_{\Delta F})^{-1}$

$$f_{j+1} = \underbrace{I\,(G^T W_e G + W_{\Delta F})}_{Q}\, f_j + \underbrace{(G^T W_e G + W_f + I\,(G^T W_e G))}_{L} e_j$$

Hence

$$\begin{bmatrix} X(Nj+N) \\ f_{j+1} \end{bmatrix} = \begin{bmatrix} D & F \\ -LH & Q - LG \end{bmatrix} \begin{bmatrix} X(Nj) \\ f_j \end{bmatrix} = \mathcal{A} \begin{bmatrix} X(Nj) \\ f_j \end{bmatrix}$$

where $\left[\begin{array}{c|c} D & F \\ \hline H & G \end{array}\right]$

$$= \left[\begin{array}{c|cccc} A^N & A^{N-1}B & A^{N-2}B & \cdots & B \\ \hline C & h_0 & 0 & \cdots & 0 \\ CA & h_1 & h_0 & \ddots & 0 \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ CA^{N-1} & h_{N-1} & h_{N-2} & \cdots & h_0 \end{array}\right]$$

Tuning Parameters:

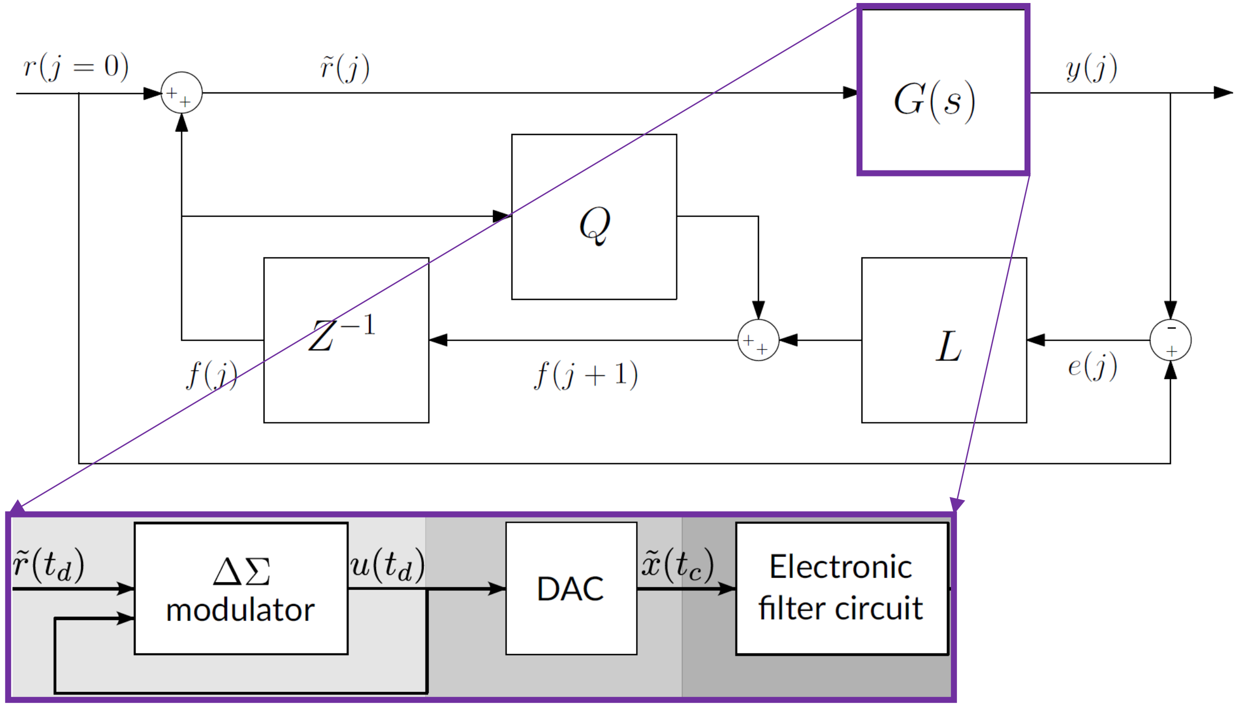
W_e (error compensation)

W_f (actuation level)

$W_{\Delta F}$ (variation in actuation)

Control Law Design Choice:

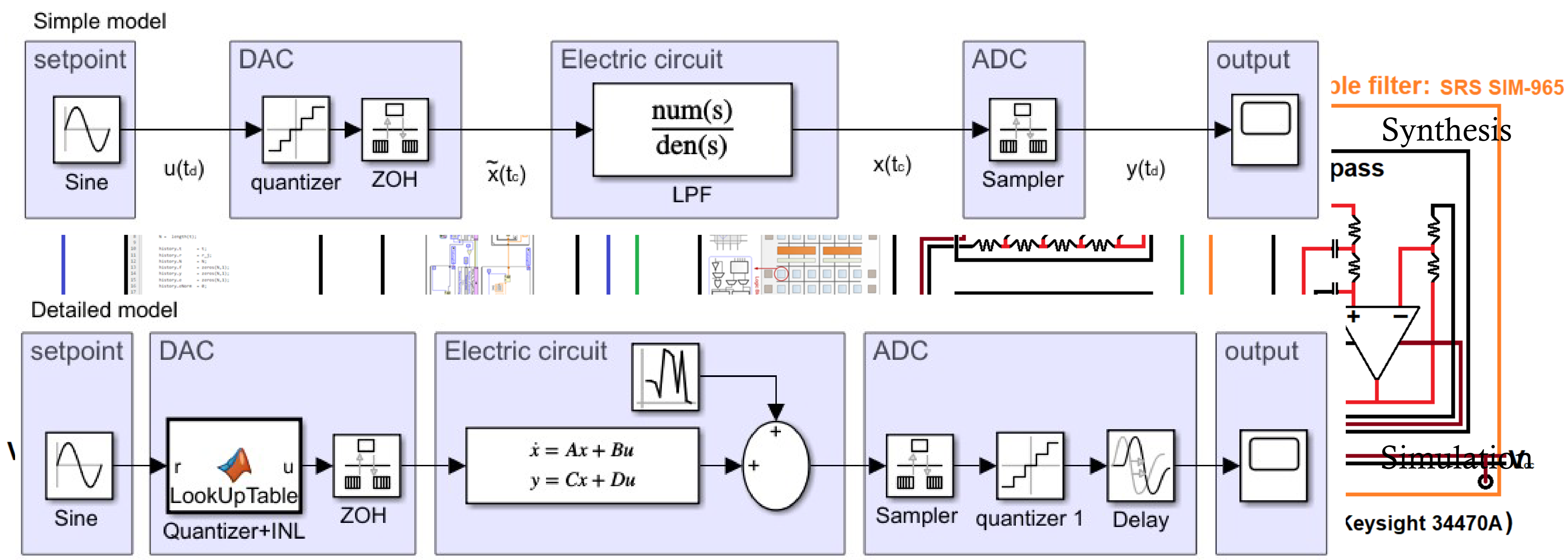
Serial Repetitive Lifted-domain Learning Control



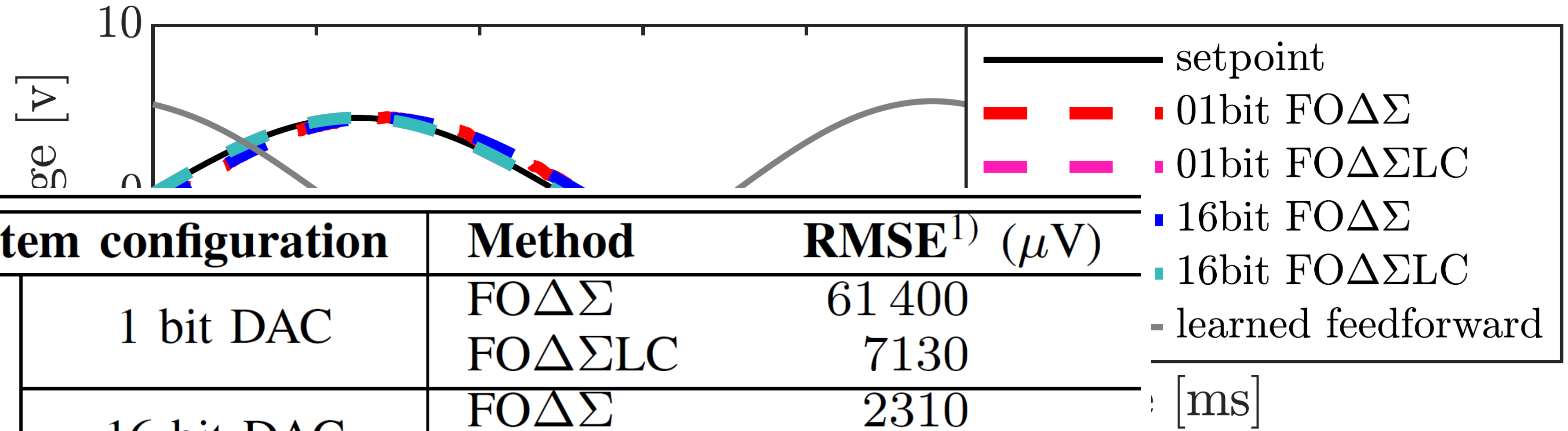
Due to the linearizing effect of the $\Delta\Sigma$ modulator over the DAC: $G(s) \approx \dfrac{{\omega_c}^2}{s^2 + \sqrt{2}\omega_c s + {\omega_c}^2}$

Hence the matrix G is obtained as the convolution matrix containing the impulse response for the dynamics of each sample in a repeating interval.

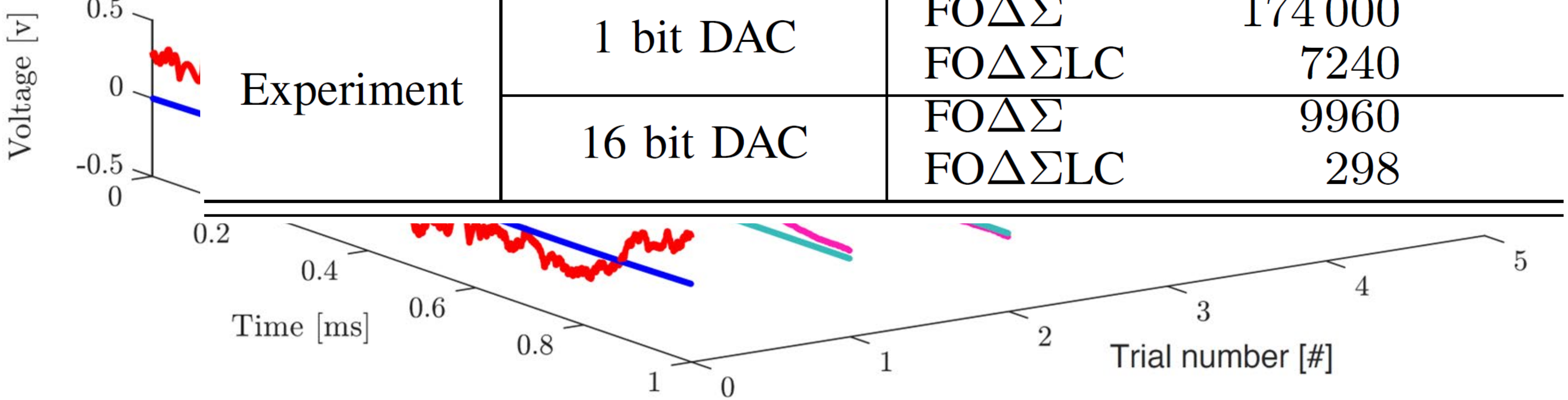
System integration and modelling



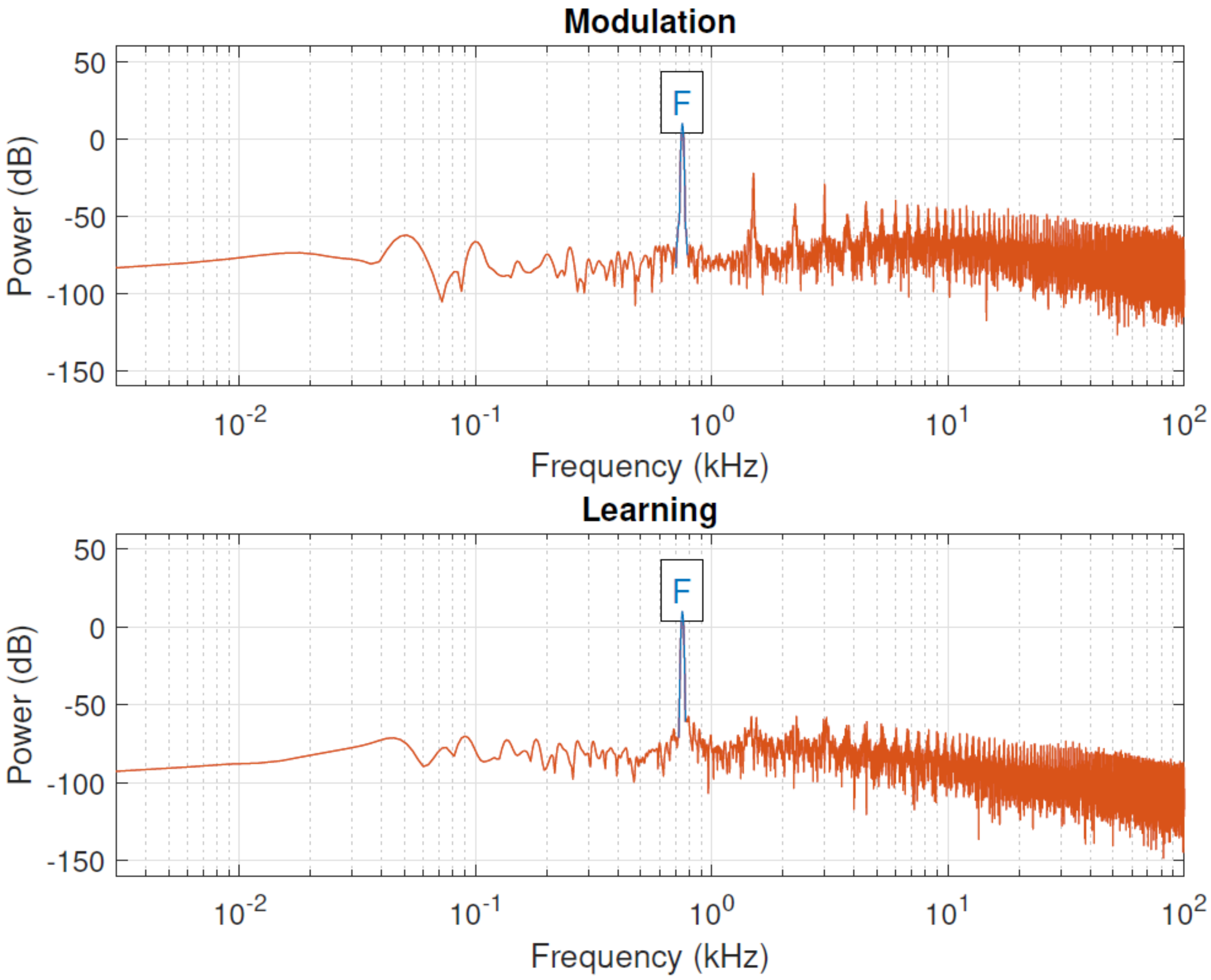
Results and Discussions



Type & System configuration		Method	RMSE[1] (μV)
Simulation	1 bit DAC	FOΔΣ	61 400
		FOΔΣLC	7130
	16 bit DAC	FOΔΣ	2310
		FOΔΣLC	109
Experiment	1 bit DAC	FOΔΣ	174 000
		FOΔΣLC	7240
	16 bit DAC	FOΔΣ	9960
		FOΔΣLC	298



Experimental Results and Performance Comparison



Type & System configuration		**ENOB**
No modulation	1 bit DAC	2
	16 bit DAC	14.7
FOΔΣ	1 bit DAC	5.9
	16 bit DAC	14.7
FOΔΣLC	1 bit DAC	9.8
	16 bit DAC	16.0

Contribution and Future work

○ Discussion		○ Recommendation	
Limitations:	- 16bit ADC measurement boundary - Extend the study to more DACs - No theoretic on analysis stability	Improvement:	- Use **DAC** in an actual system: AFF + absolute + frequency + … - ADC measurement or simulation
Possibilities:	- 95% improved RMSE performance - No manual calibration necessary - Suitable for repetitive signals	Applications:	- Digital control performance/cost - High fidelity audio system - Sinusoid linearity tests

- ○ Conclusion

  Learning control can improve the performance from a digital-to-analogue converter over traditional Delta-Sigma modulation without using complex calibrated methods.

- ○ Closing words

  1-bit DAC audio example with or without ILC:

References for external resources and visual aids

Resource:

The map of control theory:	https://engineeringmedia.com/map-of-control
R-2R resistor ladder:	https://www.electronics-tutorials.ws/combination/r-2r-dac.html
Wafer stage positioning:	https://www.micro-epsilon.com/applications/branch/Halbleiter/Positionierung-Waferstage/ https://ieeexplore.ieee.org/book/5264508
DAC card:	https://www.artisantg.com/TestMeasurement/94727-1/National-Instruments-PCIe-7852-PCIe-7852R-Mutlifuction-Reconfigurable-I-O-Device
Frequency domain learning:	https://canvas.tue.nl/courses/17897
Audiofile, “thanks for your attention”:	https://soundoftext.com/

THANK YOU